3262A
TV Sync Generator

MOS Memory Products

Description

The 3262A is a sync pulse generator that produces the necessary outputs for synchronizing television broadcast information. These outputs include Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, and Even and Odd Fields, all of which are provided in the format specified by RS170EIA Standard Output Signals. The Color Subcarrier (3.58 MHz) and the Color Burst Flag outputs are provided for color operation. All waveforms are derived from a low-voltage two-phase clock (for color operation) or a single-phase clock (for black and white operation). All outputs except the Color Subcarrier are capable of driving a TTL load directly. The Color Subcarrier is designed to drive a capacitive load. The 3262A is a monolithic integrated circuit manufactured with Isoplanar p-channel silicon gate technology.

- **COLOR OR BLACK/WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **PULSE WIDTHS DERIVED DIGITALLY**
- **OUTPUTS DRIVE TTL DIRECTLY (EXCEPT COLOR SUBCARRIER)**
- **SEPARATE VERTICAL AND HORIZONTAL RESET**

Applications

- **CAMERA LOGIC REPLACEMENT**
- **HOME TV GAMES**
- **VIDEO TAPE RECORDS**
- **VIDEO TERMINALS**

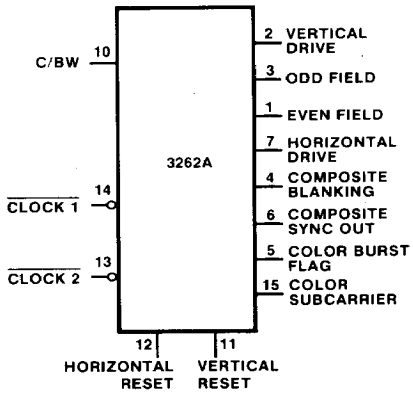
Absolute Maximum Ratings

All Inputs (Note)	−20 V to +0.3 V
V_{GG}	−20 V to +0.3 V
V_{DD} and Outputs	−6 V to +0.3 V
DC Output Current (output LOW)	<10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

All Voltages with respect to V_{SS}

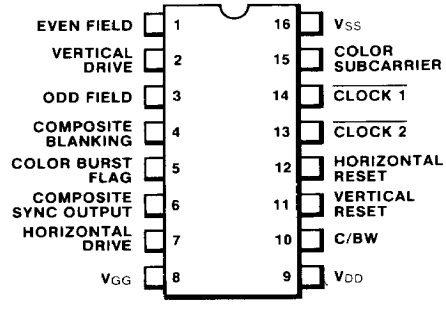
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 9
V_{GG} = Pin 8

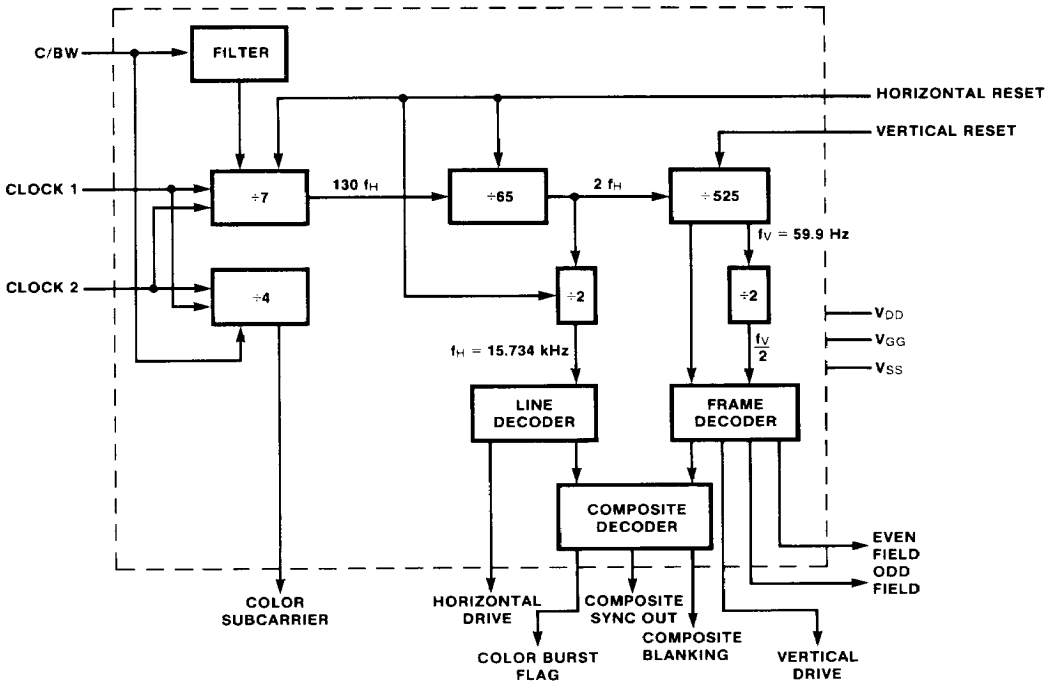
Connection Diagram
16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

Block Diagram



Functional Description

The 3262A block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is approximately a sinusodial signal. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the outputs Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3262A provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

Separate Horizontal and Vertical Reset input pins are provided to allow the 3262A to be used in systems requiring gen-lock operation. Tie Horizontal and Vertical Resets to V_{SS} when they are not used.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷4 and ÷7 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1; Clock 2 should be tied to V_{SS}. The input frequency should be 2.0475 MHz for normal operation.

C/BW when LOW also resets the Color Subcarrier. If the LOW pulse on C/BW is within the specification for t_{RS} — Color Subcarrier Reset Pulse — the color operation for the 3262A will be unaffected.

DC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to + 70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −0.8		V_{SS} +0.3	V	
V_{IL}	Input LOW Voltage	−5.0		V_{SS} −4.35	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{IHC}	Clock Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{ILC}	Clock Input LOW Voltage	−5.0 V		V_{SS} −4.35	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltage Approximate Sine wave	0.5			V_{pk-pk}	C = 10 pF to V_{DD} R = 10 kΩ to V_{DD}, Note 1
I_{IN}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		14		mA	
I_{GG}	V_{GG} Current		40		mA	

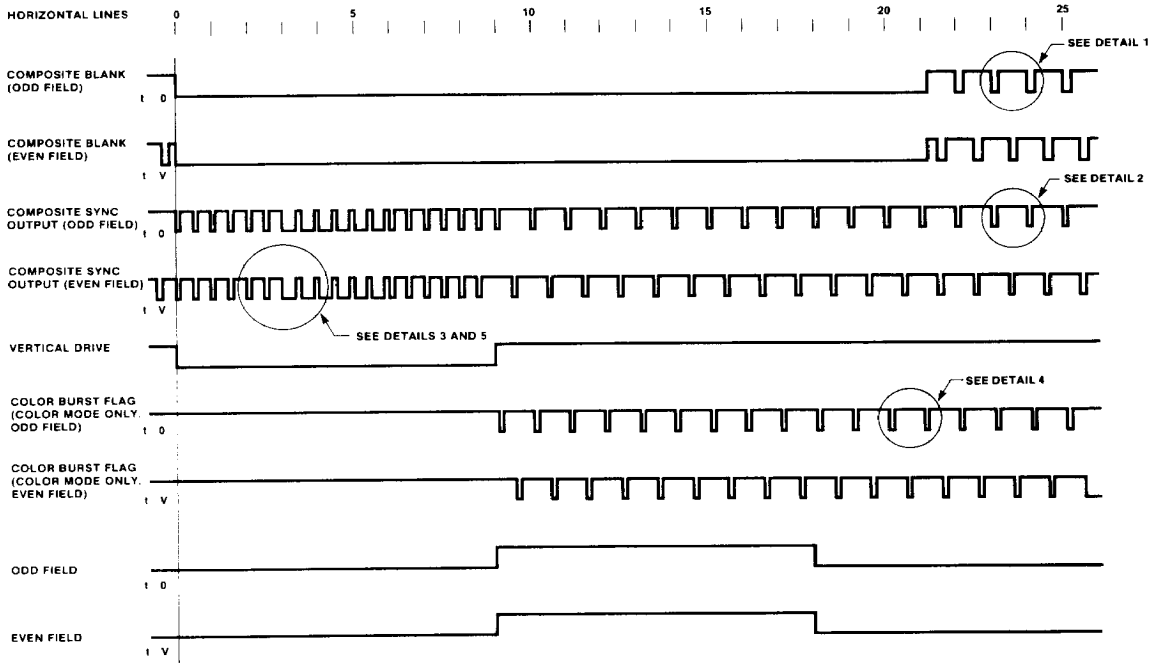
AC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to + 70°C (See Timing Diagrams)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f	Input Frequency Color	13.3	14.31818	15.4	MHz	t_r, $t_f \leq$ 5 ns
f_1	Input Frequency Black/White	1.5	2.0475	2.2	MHz	t_r, $t_f \leq$ 20 ns
t_{PW1}	B/W Clock LOW Time	200	215	230	ns	t_r, $t_f \leq$ 20 ns
$t_{\overline{PW1}}$	B/W Clock HIGH Time	200	215		ns	t_r, $t_f \leq$ 20 ns
t_{PW2}	Color Clock LOW Time	30	35	40	ns	t_r, $t_f \leq$ 5 ns
$t_{\overline{PW2}}$	Color Clock HIGH Time	30	35		ns	t_r, $t_f \leq$ 5 ns
t_{OV}	Color Clock Overlap Time			5	ns	
$t_{HR\ PW}$	Horizontal Reset Pulse Width	200			ns	t_r, $t_f \leq$ 20 ns
$t_{VR\ PW}$	Vertical Reset Pulse Width	200			ns	t_r, $t_f \leq$ 20 ns, Note 2
t_{CSR}	Color Subcarrier Reset Pulse Width	130		200	ns	t_r, $t_f \leq$ 20 ns

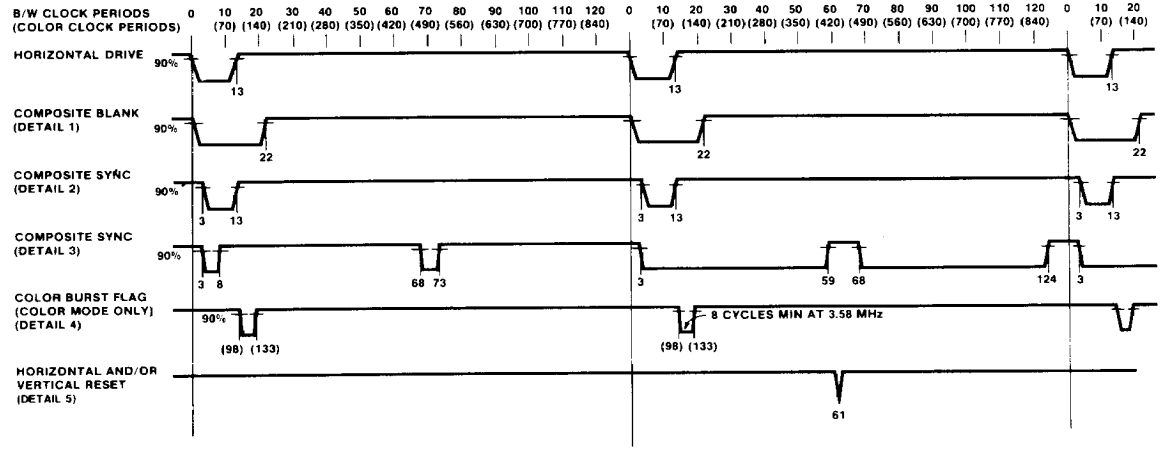
Notes

1. Subcarrier Output should be dc blocked with .01 μF before loading.
2. If t_{HR} occurs simultaneously; if t_{HR} does not occur, t_{VR} = 400 ns min.

RS170EIA Timing Diagram

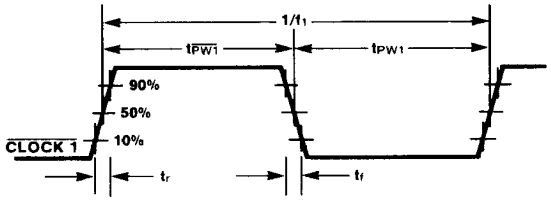


RS170EIA Timing Detail

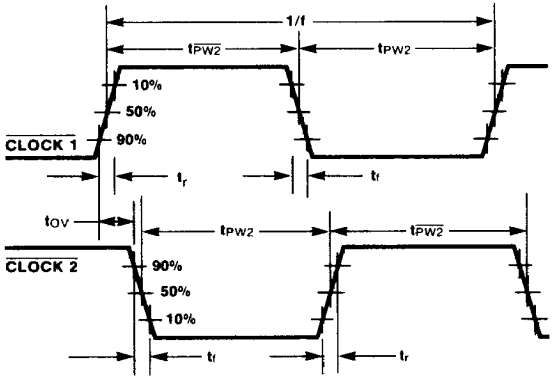


Clock Timing Diagrams

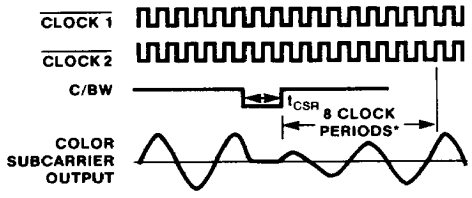
a) Black and White Clock



b) Color Clocks



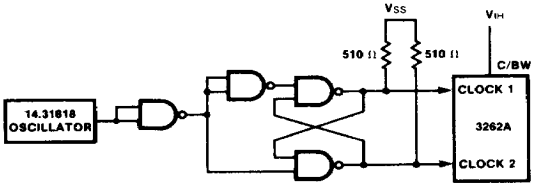
c) Color Subcarrier Timing and Reset Detail



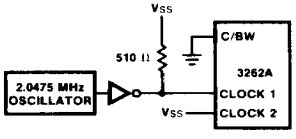
*Maximum subcarrier amplitude attained within 8 color clock periods following rising edge of C/BW.

Clock Generator Circuitry

a) Color Clocks



b) Black and White Clock



Applications

TV Camera System